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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,238	10/16/2003	Tai Anh Cao	AUS920030024US1	9411

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,238	CAO ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 7-20 is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 10/16/2003.

3. Information disclosed and list on PTO 1449 was considered.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Voss (U.S. Patent No. 6,252,818).

Regarding claim 1, Voss disclose a memory array (Figure 3) comprising:

a storage unit (325) having a number of sections, each section having a number of word lines for accessing a line of memory in the storage unit;

decoders (Figure 4, 400) coupled to respective ones of the sections (Figure 3, 310), such a decoder being operable to decode an N-bit address signal and responsively assert a signal on one of the word lines selected by the address signal (Column 4, lines 41-58) ; and

local clock buffers (Figure 4, 450, Column 4, lines 59-62) coupled to respective ones of the decoders , such a local clock buffer being operable to receive a clock signal and an address signal including M most-significant bits of the N-bit address signal and to generate a timing signal, wherein each of the decoders receives the timing signal from its respective local clock buffer and each decoder is operable to precharge responsive to a first phase of the timing signal and to evaluate the N-bit address signal responsive to a second phase of the timing signal, and wherein the local clock buffer is operable, responsive to a state of the M bits of the address signal, for selecting between holding its timing signal in a deasserted state and enabling its timing signal to follow the clock signal (Column 4, lines 58-67, Column 5, lines 1-48).

Regarding claims 2-6, Voss discloses wherein the local clock buffers are static circuitry (Figure 4), and wherein the local clock buffers are operable to receive a valid-bit signal (Column 5, lines 20-65), and the storage unit having multiple ports, wherein each of the word lines is coupled to a number of decoders (Figure 3, Column 3, lines 15-26), and wherein the word lines are for read accesses to the storage unit , and the word lines are for write accesses to the storage unit (ABSTRACT).

Allowable Subject Matter

7. Claims 7-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Claims 7-20 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Voss (U.S. Patent No. 6,252,818), and others, does not teach the claimed invention having a method for a memory array as claims 7-12 disclose and an apparatus of a memory array including a pull-up transistor coupled, by conducting electrodes, between a voltage supply and an output of one of the L inverters, the pull-up transistor having a gate coupled to the control node so that if the control node is high the pull-up transistor tends to be turned off, and if the control node is low the pull-up transistor tends to be turned on; and a isolation transistor having a gate coupled to the control node and having conducting electrodes interposed between ground and a transistor of a penultimate one of the L inverters, so that if the control node is low this tends to isolate an output of the penultimate inverter from ground, permitting the pull-up transistor to pull up an output of the penultimate inverter, which in turn tends to drive the timing signal low, and if the control node is high this permits the timing signal to follow the clock signal as claims 13-20 disclose.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER